UG-1024
6CPP6 Central Processor Panel

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UG-1024 6CPP6 Central Processor Panel
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45 Fadem Road
Springfield, NJ 07081
Phone: (973) 379-7400
Fax: (973) 379-2138
Web Site: www.qeiinc.com

Revisions

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B	Corrected RS-232 Port Speeds	January 2000
C	Formatting Update	August 2001
D	Added J8,J12 pin outs in Section 5.4	January 2006
E	Added Description of DIP 1-5	February 2012
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Contents

1 General Description 1

2 Hardware Specification 2

2.1 Communication Ports 2

3 Strapping Descriptions 5

3.1 Pluggable Jumpers 5

3.2 Strappable Jumpers 5

3.3 Dipswitches 6

4 LED Indicators 7

5 Functional Description 8

5.1 The Main Processor and Memory Section 8

5.1.1 The Processor Block 8

5.1.2 FLASH Memory 8

5.1.3 RAM Memory 8

5.1.4 Configuration Dip Switches 8

5.2 Local I/O Interface Section 9

5.2.1 Analog Panel Interface 9

5.2.2 Control Panel Interface 10

5.2.3 Status Panel Interface 11

5.2.4 QUICS I/O Interface 11

5.3 Communication Interface Section 12

5.3.1 Ports #1 and #2 13

5.3.2 Port #3 13

5.3.3 Port #4 14

5.3.4 Port #5 15

5.3.5 Additional Communication Options 15

5.4 Power Section 16

6 Typical Connection Block Diagram 17

7 Interconnection Cables 18

8 Ordering Information 18

9 Major Functions Selection 19

10 Mechanical Outline 20

11 Other Related Equipment/Programs 21

12 Other Related Documentation 21

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1 General Description

The 6CPP6 is a single-board computer incorporating specialized I/O functions for operating traditional SCADA sub-systems, such as Remote Terminal Units (RTUs). The 6CPP6 can also operate as a data concentrator in a distributed (client/server) processes environment, such as in Distribution Management Units (DMUs), Communication Interface Units (CIUs), etc. where it will be a server to a Master Station (client), and a client to the distributed process devices such as Power Line Devices, Intelligent Electronic Devices (IEDs), or other RTUs.

The central processing unit consists of a 68331 microprocessor, with dedicated program memory, RAM, and nonvolatile data memory. It also includes specialized logic which enables it to interface with standard QEI QUICS 4000 Series RTU I/O panels, and the older QUICS 3000 family plug-in cards.

Communication options include several asynchronous and synchronous data ports with bit (Serial Bit Stream, SBS) or byte-oriented data protocols, at variable baud rates. Two of these ports include the physical links necessary for a direct connection to a peripheral. The first supports a standard RS-232 interface, while the second supports an optically isolated RS-485, 2-wire interface. Additional data ports can be added by means of plug-in (32-pin DIN connectors) daughter boards, some of which offer RS-232 and/or RS-485 interfaces, or a Bell 202 type modem.

The main board also includes an RS-232 asynchronous serial Maintenance Panel interface for diagnostic and panel configuration purposes, as well as a Background Debug Monitor (BDM) port for development purposes.

Several LEDs are included to monitor different operations, such as data transmission and reception, processor heartbeat, control execution, etc.

An external single 12 volts power supply is required for operation of the 6CPP6. In addition, an external 30 VDC power supply is required, in RTUs with control functions, for activation of control relays. An internal DC/DC converter generates -12 volts for internal use and to power the -12 volts needs of other modules within the sub-system.

The 6CPP6 is mechanically compatible with its predecessors, the 6CPP4, 6CPP3 and 6CPP2 Central Processor Panels; facilitating field upgrades of existing RTUs to enhance their communication capabilities to be a server to a second Master Station, and/or be a client to multiple IEDs over several serial communication links of differing speeds and protocols.

All the operations of the 6CPP6 are under Software (program) control. The program resides in the dedicated program (FLASH) memory area. Several standard, and special, programs are available.

Before the 6CPP6 can be placed in operation, it requires setting of some hardware jumpers or switches, and proper setting of parameters in its Configuration Table. Refer to the 6CPP6 Configuration Table software for information and instructions.

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2 Hardware Specification

These specifications apply to the standard 6CPP6 alone and do not necessarily match those of a particular application incorporating this board.

ITEM	DESCRIPTION
Microprocessor	Motorola 68331 32-bit 16.78 MHz. 16-bit data bus, 24-bit address bus
FLASH, Program Memory	256 KBytes, standard; expandable up to 512 KBytes.*
FLASH, Non-Volatile	128 KBytes, standard; expandable up Data Memory to 512 KBytes.*
RAM	256 KBytes, standard; expandable up to 512 KBytes.*

** Memory requirements are controlled by the program.*

2.1 Communication Ports

Port #1 and Port #2 (JP4 & JP5)	
Interface	TTL levels, DUSART serial data, control lines, and power
Protocols	Synchronous/asynchronous, byte or bit-oriented
Bit Rate	150 to 38,400 bps
Connector	Two 32-pin DIN connectors for external daughter board

NOTE
Refer to optional daughter board documentation for appropriate specifications.

Port #3, J3 or P3 (Test Panel)	
Protocols	Asynchronous, byte-oriented
Interface	RS-232
Bit Rate	150 to 57,600 bps
Connector	P3 is female DB-9 connector, J3 is 4-pin MOLEX connector compatible with 6CPP4/3/2 Test Panel Port
Port #4, J2 (Spare)	
Protocols	Synchronous or asynchronous, byte-oriented
Interface	RS-232. Pull-up jumpers for CTS, DCD. With PTT control
Bit Rate	150 to 38,400 bps
Connector	7-pin in-line header
Auxiliary Connector J11 (Open collector current sinking)	
Number of Bits	6
Current	500 mA max per bit, 900 mW max. combined
Saturation Voltage	1.3 volts @ 200 mA
Off-state Voltage	40 volts max.
Additional Signals	External synchronous transmit/receive clocks
Connector	9-pin inline header

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Port #5, J13	
Protocols	Asynchronous or synchronous, byte-oriented
Interface	RS-485, optically isolated
Bit Rate	150 to 38,400 bps
Connector	4-terminal, plug-in terminal block
Ports #6, #7, #8 and #9 (JP6 & JP7)	
Protocols	TTL levels, parallel data and address lines, power and control signals
Interface	Synchronous/asynchronous, byte oriented
Bit Rate	150 to 38,400 bps
Connector	Two 32-pin DIN connectors for external daughter board

NOTE
Refer to optional daughter board documentation for appropriate specifications.

Analog Multiplexer Input Port, J7	
Addressability	128 points
Input Voltage	-5 to +5 VDC
Reference Points	+4.5 and -4.5 VDC
Converter	
Number of Bits	12 bits (11 bits + sign bit)
Accuracy	∀ 1 bit
Conversion Rate	50 conversions per second minimum
Common Mode Rejection	70 dB min. for power line fundamental (signal with respect to Earth)
Normal Mode Rejection	70 dB min for power line fundamental
Voltage Isolation	500 VDC analog common to logic common
Connector	16-pin IDC header
Control Output Port, J5	
Addressability	128 points (On/Off pairs)
Number Columns	16
Number Rows	8 pairs (8 Trip, 8 Close)
Drive Voltage	30 VDC, nominal
Control Pulse Duration	250 msec., default
Relay Coil Resistance	225 to 528 ohms
Safety	One relay operation at a time
Connector	34-pin IDC header
Control Power Input, J9	
Voltage Input	30 VDC, nominal
Current Input	Momentary pulse, less than 100 ma
Connector	2-pin MOLEX, miniature

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Status Multiplexer Input Port, J6	
Bit Width	16 bits
Addressability	256 points, in up to 16 standard QEI status input panels
Connector	26-pin IDC header

NOTE
Some communication protocols may limit the number of input points to a lesser number.

QUICS Bus, J4	
Interface	8 tri-state data bits, 8 XY address and 3 LSB address lines, control lines and power. Bus is compatible with QUICS 3000 family plug-in cards.
Parallel Output Bits	
Number of Bits	8, Open collector current sinking
Current	500 mA max per bit. 900 mW Maximum 8-bit combined power
Saturation Voltage	1.3 volts @ 200 mA
Off-state Voltage	40 volts max.
Connector	34-pin IDC header
Power Input, J8	
Voltage	+10.5 to +14.4 volts
Current	0.5 Amps DC max. Does not include power drawn by I/O panels, or external loading of the -12 VDC output.
Connector	3-pin MOLEX
-12 volts Output, part of J8	
Voltage	-11 to -13 volts
Current	200 mA max. load
Connector	Part of J8
Environment	
Temperature	**0 to +70ºC**
Humidity	5 to 95% @ +70ºC, non-condensing

Physical Dimensions
11.63 in x 10.35 in x 2.25 in Mechanically interchangeable with the 6CPP2, 6CPP3, and 6CPP4
Weight
1 3/4 lbs.

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2 Strapping Descriptions

Some hardware and firmware options are selected by individual pluggable jumpers, or dip switches. Individual pluggable jumpers are designated JP2, JP3, and JP14; while JP8 and JP9 are two groups of parallel pins, where option selection is made by strapping (jumpering) one pair of pins. 8-position dipswitches are designated S1 and S2.

2.1 Pluggable Jumpers

JUMPER REF DESIGNATION	FUNCTION
JP2	+12V pull-up resistor for CTS on Port 4
JP3	+12V pull-up resistor for DCD on Port 4
JP14	Watchdog timer jumper IN = Watchdog timer enabled OUT = Watchdog timer disabled

2.2 Strappable Jumpers

PIN GROUP	FUNCTION
JP8	Port #2 bit rate selector for bit-oriented protocol. Bit rate is as follows:

JP8 Jumper	Bit Rate (Bps)
1-2	37.5
3-4	75
5-6	150
7-8	600
9-10	1200
11-12	2400
13-14	4800
15-16	9600
17-18	19200
19-20	38400

JP9	Port #1 bit rate selector for bit-oriented protocol. Bit rate options are the same as for JP8, above.

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2.3 Dipswitches

Dipswitch usage and/or function is firmware dependent. In most application S2 switches are used to set the least significant bits (1 to 255) of the station address. Reference should be made to the specific system documentation (Parts Lists, Point Assignment Charts, etc.) for their usage or function description.

<table>
<tr><th>SWITCH BANK</th><th>FUNCTION</th></tr>
<tr><td>S1</td><td>Switch #8 is used to transfer a factory default configuration table to the non-volatile data memory block.

WARNING
Setting S1, switch #8 to ON, turning power OFF, and back to ON will transfer the Factory Default Configuration Table into the non-volatile data memory block. This will over-write and destroy any existing configuration table.

Switch #7 is used to temporarily set the Test Panel port (Port #3) for main program downloading.

Switch #5 is used to disable the optional 6NIA. If no 6NIA is present, switch 5 must be ON.

All other switches on the S1 bank are reserved for future assignment</td></tr>
<tr><td>S2</td><td>The switches in this switch bank are used to set the LSB of the station address, as follows:
<table>
<tr><th>Switch</th><th>Value</th></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>2</td><td>2</td></tr>
<tr><td>3</td><td>4</td></tr>
<tr><td>4</td><td>8</td></tr>
<tr><td>5</td><td>16</td></tr>
<tr><td>6</td><td>32</td></tr>
<tr><td>7</td><td>64</td></tr>
<tr><td>8</td><td>128</td></tr>
</table></td></tr>
</table>

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3 LED Indicators

All LED's are physically placed in a straight line along one edge of the panel. LEDs are separated by group according to function. For example, Port #1 LEDs are slightly separated from Port #2 LEDs, etc. LEDs are labeled as follows:

LED	FUNCTION	INDICATION
D46	+12VDC	Monitors the +12 VDC power input
D47	VCC	Monitors the VCC (+5 VDC power supply)
D48	-12VDC	Monitors the -12 VDC power supply
D49	PORT 1 TX	All communications ports on the 6CPP6 (with the exception of Test Panel Port Port #3) have LEDs attached to the TX, RX, and PTT/RTS Lines. Each LED provides a visual indication of TX and RX data and Push-to-Talk/RTS control to/from the respective port.
D50	PORT 1 RX	
D51	PORT 1 RTS	
D52	PORT 2 TX	
D53	PORT 2 RX	
D54	PORT 2 RTS	
D55	PORT 4 TX	
D56	PORT 4 RX	
D57	PORT 4 RTS	
D58	PORT 5 TX	
D59	PORT 5 RX	
D60	PORT 5 RTS	
D61	HEARTBEAT/RESTART	This LED provides visual indication that the microprocessor is running. The LED flashes at a constant rate during normal operation.
D62	CONTROL EXECUTE	LED provides a visual indication when a Relay Control is energized.
D63	SPARE	A software controllable LED is provided for misc. applications.

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4 Functional Description

The 6CPP6 Central Processor Panel consists of four major functional sections: the main processor and memory section, the local I/O interface section, the communications section, and the power section

The following paragraphs give a brief description of the operation of each of these four sections.

4.1 The Main Processor and Memory Section

The main processor and memory section control the entire operation of the 6CPP6 and consists of the following blocks:

- The Processor
- FLASH memory
- RAM memory
- Configuration dip switches

4.1.1 The Processor Block

The Processor block consists of the microprocessor, Motorola 68331 32-bit 16.78 MHz, the 16-bit data bus and the 24-bit address bus, the clock generator, watch-dog timers, and two 64-pin DIN connectors to extend the data and address buses, for future expansion.

Under program control, the microprocessor services all the I/O and communications functions.

4.1.2 FLASH Memory

FLASH memory is divided into two separate blocks:

- The Program Memory block, which is normally a 256-KByte block with provisions to be expanded up to 512-KBytes. This memory section is reserved for program storage.
- Non-Volatile Data Memory block for storage of the processor configuration tables. This is a 128-KByte memory block and has provisions to be expanded up to 512 KBytes.

4.1.3 RAM Memory

RAM memory consists of a 256-KByte block and can be expanded up to 512-KBytes. RAM is the temporary storage area where program variables, intermediate process variables and data from digital and analog input points (status, analogs, accumulators, etc.) are stored.

4.1.4 Configuration Dip Switches

The 6CPP6 has two 8-switch dipswitch banks, S1 and S2. These switches are used to configure some basic parameters. Dipswitch usage and/or function are program dependent.

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4.1.4.1 S1 Dip Switch Bank

S1, switch #8 is used to transfer a **factory default configuration table** to the non-volatile data memory block on 6CPP6 panels that have never before been configured. This factory default configuration table ONLY configures the parameters needed to enable the Test Panel communications port #3, J3/P3, as follows:

9600 bps, 8 data bits, 1 start bit, 1 stop bit, no-parity, and XON/XOFF flow control

Switch #7 is used to temporarily set the Test Panel port (Port #3) for main program downloading (FLASH Loader mode).

All other switches on the S1 bank are reserved for future assignment.

WARNING
Setting S1, switch #8 to ON, turning power OFF, and back to ON will transfer the Factory Default Configuration Table into the non-volatile data memory block. This will over-write and destroy any existing configuration table.

4.1.4.2 S2 Dip Switch Bank

In most applications the switches on the S2 switch bank are used to set the least significant bits (1 to 255) of the station address. Some communications protocols may limit the station address to a lower number. For example, the QUICS 4000 protocol limits the station addresses to 63. Reference should be made to the specific system documentation (Parts Lists, Point Assignment Charts, etc.) for their usage or function description.

4.2 Local I/O Interface Section

The local I/O interface section provides the necessary circuitry to properly service the standard QUICS 4000 series Remote Station I/O panels and in addition includes a data and address bus to service some of the QUICS 3000 family of plug-in cards.

The local I/O interface section consists of the following interfaces:

- Analog Panel Interface (API)
- Control Panel Interface (CPI)
- Status Panel Interface (SPI)
- QUICS I/O Bus Interface (QIB)

4.2.1 Analog Panel Interface

The Analog Input Panel Interface (API) enables the 6CPP6 system to sample differential analog input signals that are wired to the local Analog Input Panels (6AIP1). Under program control, this API selects one of up to eight 6AIP1s and one of the sixteen input points in each of these panels, for a total of 128 analog inputs. The API also includes two fixed reference points (-4.5 and +4.5 VDC). If these two reference points are used, they must be included as two of the 128 analog points.

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The selected analog input, in the range of 0 to ∀5 VDC, is digitized by the A/D converter into a 12-bit signed value (11-bit plus sign). This value is stored in RAM for further processing and subsequent transmission to the "client".

Unlike the other panel interfaces, where the isolation is done at the panels themselves, the API has its own isolation on board. A DC/DC converter provides the necessary power supply and isolation for the 6AIP1s, while opto-isolators are used to provide isolation for the logic signals.

A 16-pin IDC header, J7, is used for the connections to the 6AIP1 panels through a 16-conductor ribbon cable. Signals in this connector include:

- 3 panel select lines
- 4 point select lines
- 1 enable line
- 2 ∀15 VDC isolated power lines
- 3 common (analog ground)
- 2 analog signal lines
- 1 acknowledge line

4.2.2 Control Panel Interface

The Control Panel Interface (CPI) provides the means for the system to momentarily energize external relays (control output points) in response to control commands received from the "client", or locally generated from internal processes.

The CPI has the capability of controlling up to 256 momentary relays, or 128 control point outputs.

Each control output point consists of one pair of complementary command functions, such as OPEN/CLOSE, SET/RESET, etc. Each control output point is normally equipped with an external pair of momentary relays, or a single electrically or mechanically latching relay. These external relays are arranged, or grouped, in external control point output panels. There are several control point output panel arrangements, with the 6COP1 being the most commonly used (most control output panels are groupings of eight control output points, however some may have only four control output points).

The CPI executes a command by selecting a single external relay, then energizing its coil for a pre-defined period of time. To do this, the CPI provides 16 current source lines and 16 current sink lines. The current source lines (8 trip and 8 close) act as a relay select, while the current sink lines act as a panel select (group of 8 control output points). Together, they complete a current loop that energizes the selected relay.

The CPI includes circuitry to insure that only one output relay is energized at a time. If more than one relay is being energized, because of component failure, a selected-row/column detector aborts the command.

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An external 30 VDC power source is required for relay operation. A 2-pin miniature MOLEX connector, J9, is provided for this input.

A 34-pin IDC header, J5, is used for the connections to the control point output panels (i.e., 6COP1, etc.) through a 34-conductor ribbon cable. Signals in this connector include:

- 16 column lines (panel selects)
- 8 trip lines (relay selects)
- 8 close line (relay selects)

4.2.3 Status Panel Interface

The Status Panel Interface (SPI) provides the means for the system to sample digital input data points. These digital points can be configured in various ways, for example:

- Individual Status Points (on/off indications)
- Accumulators, where the pulse count reflects a value.
- Pulse Duration Input (PDM), where the pulse width reflects a value

The SPI is capable of monitoring up to 16 individual Status Input Panels (6SIP1) each containing 16 inputs, for a total of 256 individual digital input points. Some communication protocols, may limit the number of input points defined as status points to a lesser number of points.

The SPI, under program control, reads the state (0 or 1 value) of the digital points in the selected 6SIP1 panel. This value is stored in RAM for further processing and subsequent transmission to the "client".

A 26-pin IDC header, J6, is used for the connections to the 6SIP1 panels through a 26-conductor ribbon cable. Signals in this connector include:

- 5 panel select lines
- 16 data bit lines
- 1 LATCH-EN line (turns on the V1 LED on the 6SIP1 panel)
- 1 SIP-ACK line (Status Panel Acknowledge)
- 1 +12 VDC power line
- 2 power common lines

4.2.4 QUICS I/O Interface

The QUICS I/O Bus (QIB) is a 6CPP6 interface that provides support for some of the QUICS 3000 family of cards. These cards include the 6DA, 6DD, 6DO, 6SP, 6ST, 6TM, and 6UF. It also provides support for the 7BI1 card. This interface was designed to allow for backward capability with older QUICS 3000 systems.

The QIB interface provides the QUICS 3000 XY address lines which are used as the card select lines. Three low order address lines allow for additional function address decoding by the individual cards. The data bus is 8 bits wide and bi-directional (tri-state). A R/W line

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controls direction of the data bus and a WP (Write Pulse) is used for gating purposes. An interrupt line (IRQ) enables this bus to generate a hardware interrupt directly to the 6CPP6's CPU.

A 34-pin IDC header, J4, is used for the connections to the QUICS 3000 cards (i.e., 6TM2, 6DA1, etc.) through a 34-conductor ribbon cable. Signals in this connector include:

- 8 data lines
- 8 XY address lines (card selects)
- 3 low-order address lines (card function enables)
- 1 card bank select line
- 1 R/W line
- 1 WP line
- 1 IRQ interrupt line
- 1 +12 VDC power supply line
- 2 power supply common lines

A group of 8 Open-collector parallel output points (each capable of sinking up to 300mA at 30 Volts) is provided on the same connector.

4.3 Communication Interface Section

The 6CPP6 panel contains circuitry for five serial communication ports. Four of these ports are capable of handling synchronous or asynchronous communication protocols, at various baud rates. Optionally, the 6CPP6 also provides support for four additional serial communication ports. All communication ports may be configured to provide hardware and/or software XON/XOFF handshaking.

The following are descriptions of the communications ports usage in a typical SCADA system including, their physical interfaces and options available to them.

The five serial ports on the 6CPP6 panel, and their currently assigned functions are:

Port #1: General Purpose

- Requires Daughter board for physical interface
- Bit/Byte Oriented
- Synchronous – Asynchronous
- 150 - 38,400 bps

Port #2: General Purpose

- Requires Daughter board for physical interface
- Bit/Byte Oriented
- Synchronous – Asynchronous
- 150 - 38,400 bps

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Port #3: Maintenance Panel

- RS-232 interface
- Byte Oriented
- Asynchronous
- 150 - 57,600 BPS

Port #4: General Purpose

- RS-232 interface
- Byte Oriented
- Synchronous - Asynchronous
- 150 - 38,400 bps

Port #5: Normally used to communicate with LEDs

- RS-485 opto-isolated transceivers on board
- Byte Oriented
- Synchronous - Asynchronous
- 150 - 38,400 bps

4.3.1 Ports #1 and #2

These two ports are normally assigned to be the main communication link(s) to one or more Master Stations (clients). Both of these ports have identical functionality and capabilities. They can support synchronous and asynchronous, bit and byte oriented communication protocols at various baud rates. Neither of these ports have a direct physical link to the outside world, but rather they interface to a pair of connectors, JP4 and JP5 which allows for several different physical layer options on several different optional daughter boards. Daughter boards that may be installed on JP4/JP5 are the 6LAP2-1 or the 6LAP4-1. *Refer to their individual User's Guides.*

Along with the transmit, receive and control signal lines for the serial links of ports #1 and #2, there are additional data, address, select and control lines which provide the necessary support for future, or special, interface daughter boards.

Each of these two ports have status indicator LEDs on their transmit, receive and Request To Send (RTS/PTT) control lines.

4.3.2 Port #3

This port utilizes the Serial Communication Interface built into the 68331. It is called the Maintenance Panel Port because its main function is to provide a clean, simple interface to the test technician, allowing him to control and query the status of the 6CPP6 or its data. This port is also used for downloading software, configuration tables, etc. These procedures are normally performed from a Lap Top PC (6TP4 Test Panel).

This is an RS-232 interface port supporting only software handshaking. Connections can be made to it through a 4-pin Molex connector (J3) or through a standard DB9 connector (P3) and one-to-one Modem cable. The 4 pin Molex connector is compatible with the cable normally supplied with the 6TP4 Test Panel.

WARNING
Test Panel Port #3 configuration (i.e., speed, etc.) must match the port configuration on the 6TP4.

4.3.3 Port #4

This is an RS-232 interface port and can be configured to handle any mode or protocol supported by the 6CPP6 program.

A 7-pin in-line header, J2, is used for connections to an external communications device, such as an RS-232 interface modem or radio. RS-232 signals in this connector are:

PIN #	SIGNAL
1	CTS
2	RTS
3	DCD
4	TXD
5	RXD
6	COMMON
7	PTT

Jumpers JP2 and JP3 can be installed to pull up the CTS and DCD lines and force them to the enable state, if needed.

The Push-To-Talk (PTT) signal can be used to key an external radio, if needed. This output is in the form of an open collector output.

This port has status indicator LEDs on its transmit, receive and Request To Send (RTS/PTT) control lines.

In Load Management systems, this port works in conjunction with the Distributed Load Management Synchronous Communications Modem Control Port (DLMSCMC). The DLMSCMC port consists of six open collector signals capable of sinking up to 300 mA at 30 volts, along with two clock lines.

A 9-pin in-line header, J11, is used for connections to the Load Management Distribution Line Transceiver (7DLT1). Signals on this connector are:

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PIN #	SIGNAL
1	COMMON
2	DLM-ML0 (bit0)
3	DLM-ML1 (bit1)
4	RCLK
5	TCLK
6	DLM-ML2 (bit2)
7	DLM-ML3 (bit3)
8	DLM-ML4 (bit4)
9	DLM-RESET (bit7)

4.3.4 Port #5

This is an RS-485 interface port normally used to communicate with Intelligent Electronic Devices (IEDs). This port conforms to the RS-485 specification and is suitable for direct wiring with external IEDs. High-speed opto-couplers provide isolation, while fast Schottky, Zener diodes, and surge suppressing capacitors clamp any input voltage transient and noise to chassis ground.

This port is capable of supporting multiple devices over a single twisted pair of wires. The choice of IED communication protocols is entirely under software control.

A 4-terminal plug-in terminal block, J13, is used for connections to the external IEDs. RS-485 signals on this terminal block are:

TERM. #	SIGNAL
1	SHIELD
2	DATA B-
3	SHIELD
4	DATA A+

NOTE
A 220 ohm terminating resistor is included on board.

4.3.5 Additional Communication Options

There is a second pair of 32-pin DIN connectors, JP6 and JP7, which contain power, 8 address lines, 8 data lines, R/W, QUART-CS, CINT3, and RESET signals. These connectors provide a general purpose bus interface to facilitate the addition of up to four communication ports on an optional daughter board.

A daughter board that may be installed on JP6/JP7 is the 6LAP3-1. Refer to the 6LAP3-1 User's Guide.

WARNING
Connector pair JP6/JP7 is not compatible with connector pair JP4/JP5. Daughter boards designed for installation in the JP4/JP5 connector pair must not be installed in the JP6/JP7 connector pair, or vice versa.

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In addition to all the communication ports described above, Port #0 (JP1), the Background Debug Monitor (BDM) port is included. This port is assigned for development purposes and factory use only.

4.4 Power Section

The 6CPP6 operates from a single 12 VDC power input. The following voltages are internally generated from this 12 VDC supply:

- -12 VDC for internal and external use is generated by a non-isolated DC/DC converter.
- +5 VDC for internal use is generated by a voltage regulator.
- +5 VDC isolated, for use in the RS-485 interface is generated by an isolated DC/DC converter.
- ∀15 VDC isolated, for use by the Analog Panel Interface is generated by an isolated DC/DC converter.

A 3-pin MOLEX connector, J8, is used to bring 12 VDC into the 6CPP6. Pin #1 is used for +12VDC input while pin #2 is used for 0 VDC. Pin #3 in this connector is used as the source for the -12 VDC supply for external use.

In addition, a 2-pin miniature MOLEX connector, J12, is provided to be used as an auxiliary +12 VDC source for external use. Pin #1 is used for 0 VDC and pin #2 is used for +12 VDC.

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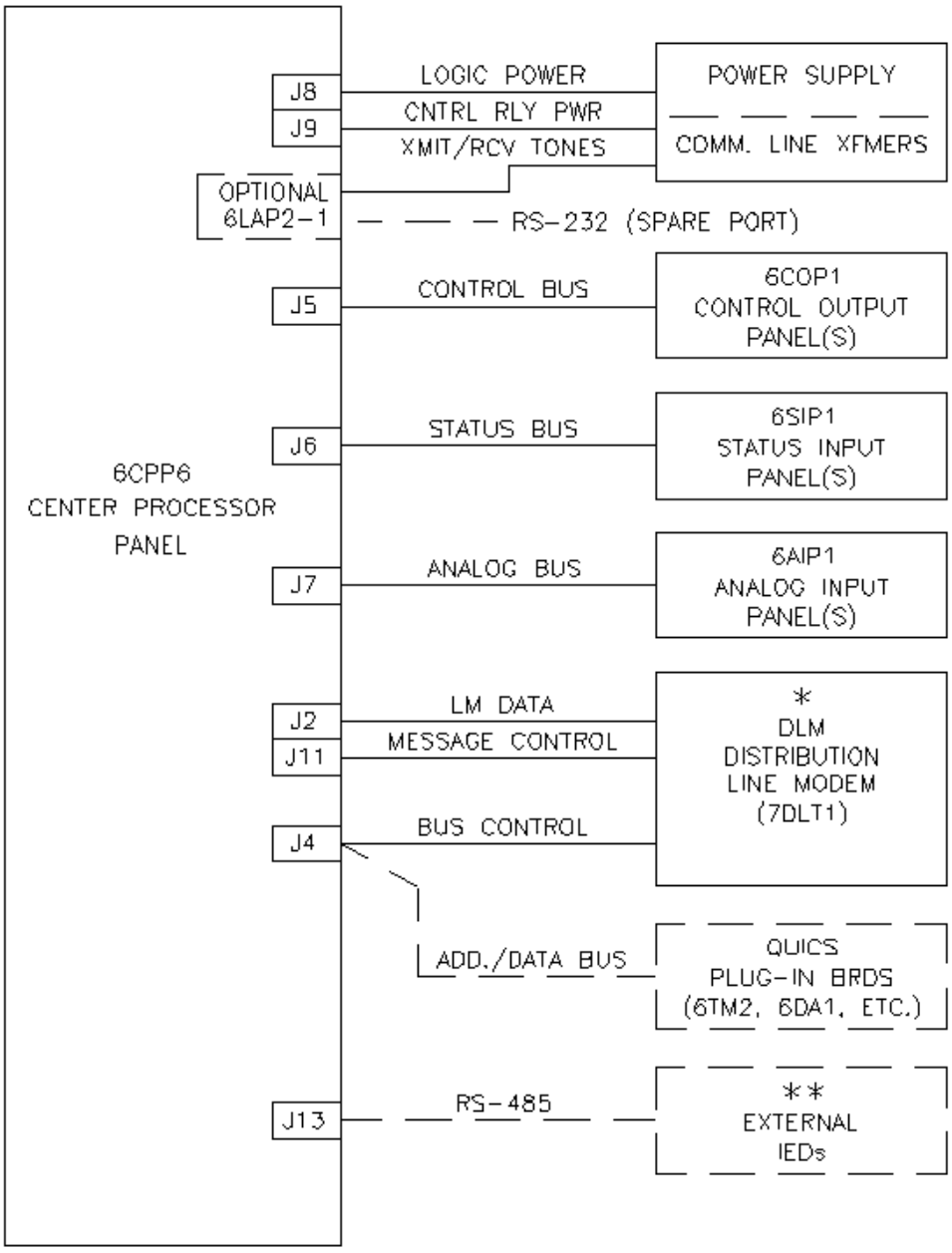
5 Typical Connection Block Diagram



* SYSTEMS WITH LOAD MANAGEMENT FUNCTION, ONLY.

** SPECIAL APPLICATION SYSTEMS, ONLY.

6 Interconnection Cables

Some typical interconnecting cable part numbers for "standard" RTU applications are listed below, all cables must be ordered separately. This is only a partial list. For RTUs with non-standard or special applications, refer to the documentation supplied with those systems.

CABLE PART #	FUNCTION	FROM	TO
30-057915-XXX	Analog Bus	J7	1st Analog Input Panel
30-057916-XXX	Control Bus	J5	1st Control Output Panel
30-057917-XXX	Status Bus	J6	1st Status Input Panel
30-058402-XXX	Power Input	J8	Power Supply Panel
30-057922-XXX	Control Pwr.	J9	Power Supply Panel
30-057925-XXX	Communications	6LAP2	Power Supply Panel
30-057916-XXX	Data Bus	J4	Distribution Line Modem or QUICS Plug-in Boards
40-057101-XXX	LM Data	J2	Distribution Line Modem
40-057133-XXX	Message Cntrl	J11	Distribution Line Modem
40-057582-007/XXX	Serial Comm.	J2	External Device (6PTM2, modem, etc.). May require an RJ45 to DB-9 or DB-25 adapter
40-057457-001	Serial Comm.	J3	6TP4 Test Panel
10-057126-001	Serial Comm.	P3	6TP4 Test Panel

"XXX" Indicates cable length option.

7 Ordering Information

Full ordering information includes a panel assembly Part Number and a panel assembly Model Designation.

The panel assembly Part Number is a number in the form of 40-057552-YYYY, where -YYYY is the number specifying major functions assembly options per drawing of 8.1 (found in this section).

The Model Designation is a generic alpha-numeric sequence of characters specifying optional strapping information, and is in the form of 6CPP6-A/MOD XX, per drawing of 9., also in the next pages.

In addition to this, the Central Processor Panel requires a Program Link. The Program Link number is in the form of 80-XXXXXX-YYY#, where -XXXXXX is the base program link, -YYY is a configuration option, and # is the current revision level. To specify the required Program Link, please refer to the System Parts Lists, and in particular to the Parts List for the specific Remote Station Assembly.

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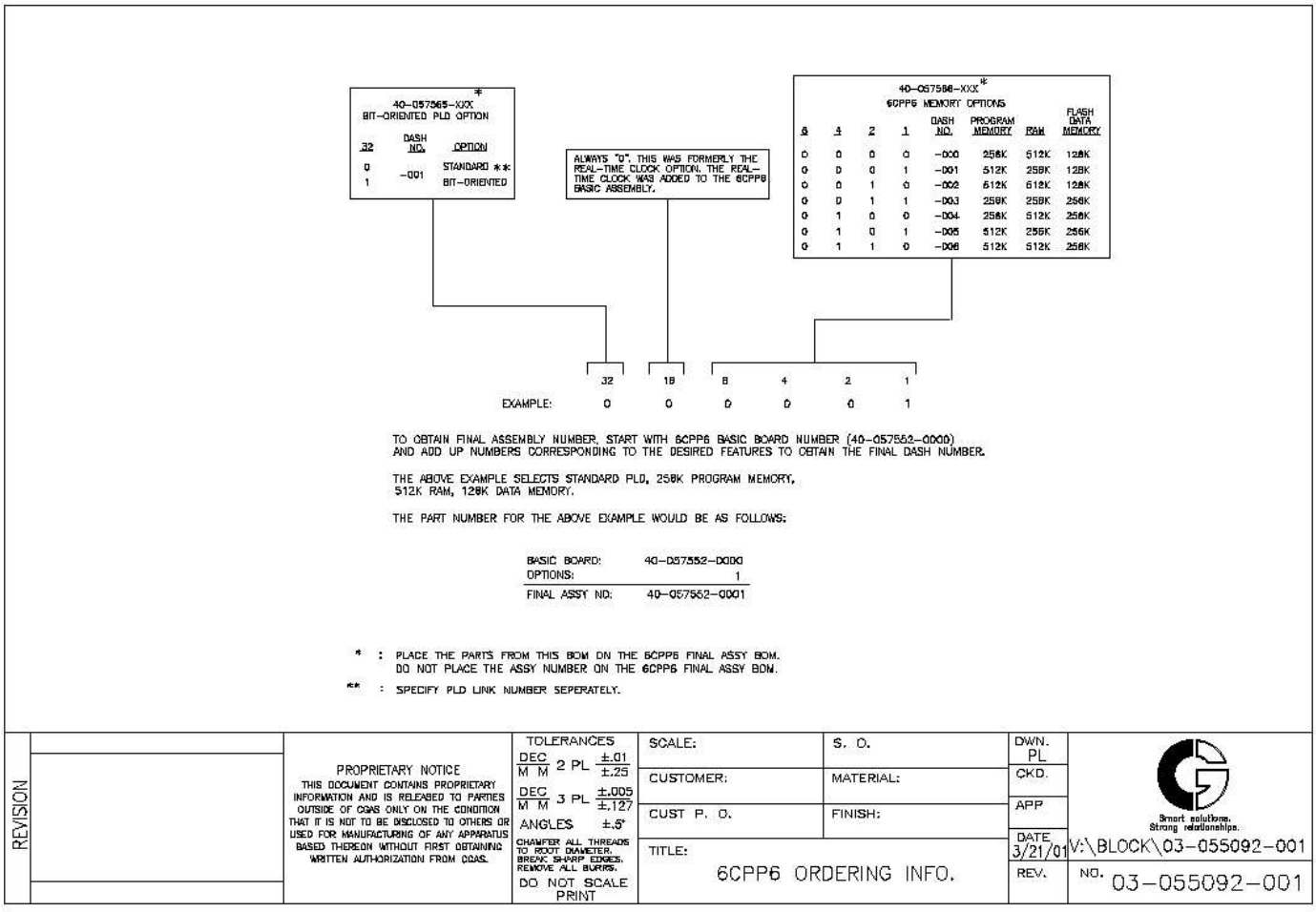
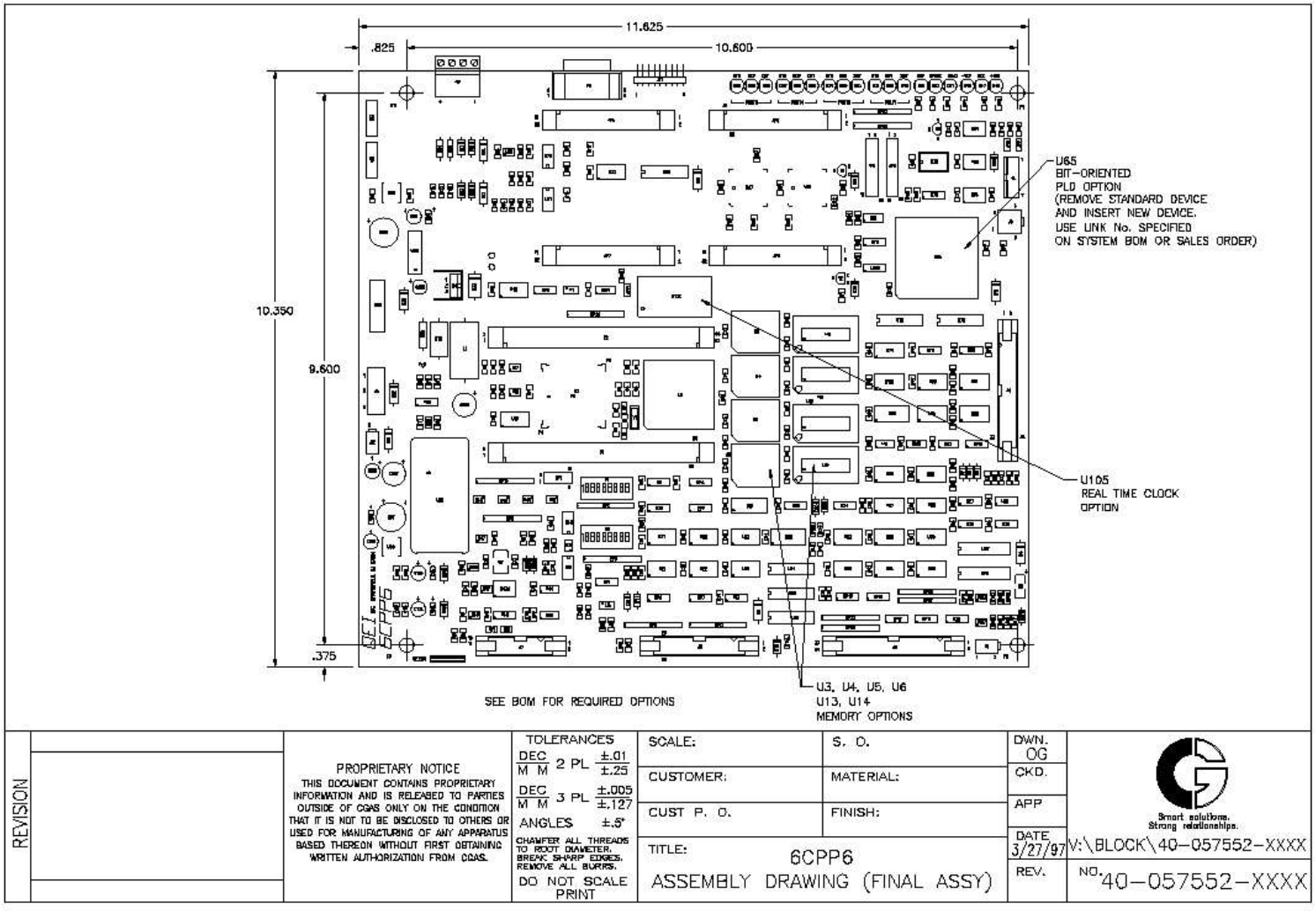
NOTE
Not all the RTUs in a system have to be equipped with the same Program Link. RTUs performing special functions may have different Program Links.

8 Major Functions Selection



9 Mechanical Outline



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10 Other Related Equipment/Programs

Model No.	Description	QEI Part #
6LAP2-1	LAN ADAPTER PANEL (Dual-Port Daughter Board, one port Bell 202 Modem, second port RS-232 Interface)	40-057558-001
6LAP3-1	LAN ADAPTER PANEL (Four-Port Daughter Board, three RS-485 or four RS-232)	40-057564-001
6LAP4-1	LAN ADAPTER PANEL (Dual-Port Daughter Board, two RS-232 ports)	40-057575-001
RPMC1-1	6CPP6 RTU Configuration Software (6CPP6 Release 1)	80-000050-001

11 Other Related Documentation

Doc No.	Document Name
UG-1025	6LAP3-1 LAN ADAPTER PANEL, Four-Port Daughter Board User's Guide
UG-1026	6LAP4-1 LAN ADAPTER PANEL, Dual-Port Daughter Board User's Guide
UG-1027	6LAP2-1 LAN ADAPTER PANEL, Dual-Port Daughter Board User's Guide
UG-1032	6LAP5-1 LAN ADAPTER PANEL, Dual-Port Daughter Board User's Guide
TP-801	QEI QUICS 6TP4 TEST PANEL INSTRUCTION MANUAL

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